

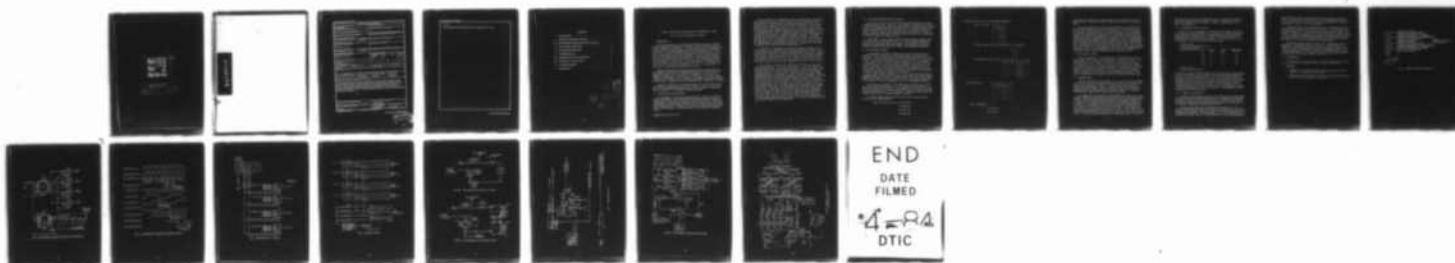
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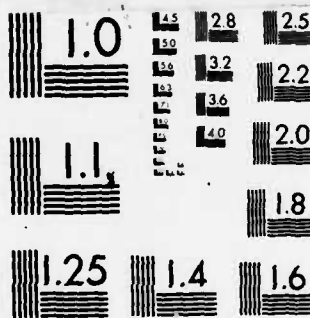
A CIRCUIT DESIGN FOR MULTIPLEXED DIGITAL CORRELATION AT 1/1
60 MHZ(U) NAVAL RESEARCH LAB WASHINGTON DC
J H LAYNO ET AL. 06 MAR 84 NRL-MR-5276

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<p>Methods have recently been developed to improve the speed of digital correlators by application of time division multiplexing techniques. Using one such method, a correlator circuit may be constructed in which several multiplexed correlators are parallel loaded with data in a sequential manner and an overall correlation output is determined by properly sampling the outputs of each multiplexed correlator. The design of a single 64×4 bit multiplexed correlator is presented. Data selection circuitry to form the correct correlation from several such correlators is described. Design considerations arising from the correlator's desired operational rate of 60 MHz are discussed.</p>				
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A CIRCUIT DESIGN FOR MULTIPLEXED DIGITAL CORRELATION AT 60 MHz

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A CIRCUIT DESIGN FOR MULTIPLEXED DIGITAL CORRELATION AT 60 MHz

John H. Layno and Lawrence M. Leibowitz

I. INTRODUCTION

Several approaches to time division multiplexing of digital correlator devices, whereby k operations are overlapped in time, have been developed by NRL as described in Reference 1. Previous laboratory work has demonstrated the basic logical concepts behind the parallel-load scheme for multiplexed correlation. An N -bit multiplexed digital correlator operating at a clock rate f can be attained using k N/k -bit correlator devices with clock rate f/k and thus accomplish k -times speed improvement. Where pre-synchronization with the input signal data is not available, k such multiplexed correlator circuits are required with proper selection of correct synchronized outputs formed by means of a data selector. This report discusses considerations for optimal speed operation and describes the design of a multiplexed correlator circuit for subsequent implementation of 64×4 bit correlation at a clock rate of 60 MHz using the parallel-load method.

Because satisfactory analog switching devices could not be found for such high-speed operation, the design presented uses the TRW TDC1023J 64-bit long digital output correlator described in Reference 2. This device is capable of operation at clock rates up to 20 MHz but 15 MHz operation was assumed in this design. At any one time, the TDC 1023J 7-bit output presents a sum equal to the number of bit positions in agreement between the correlator device's 64-bit A register and its corresponding 64-bit reference (R) register.

Sections I through IV of this report discuss the circuit design for the high speed multiplexed digital correlation process. Sections V and VI deal with the other experimental hardware that will be necessary for implementation and operation of a working multiplexed correlator.

II. CIRCUITRY FOR 60 MHz OPERATION

In this design, the two input signal generators assumed for the multiplexed correlator are a Tau-Tron MG-302 Data Generator, which provides the 60 MHz clock and data, and a Rutherford B-15 Pulse Generator for single shot triggering of the synchronous loading and correlating processes. Though the pulse generator can be replaced by other models, care must be taken in replacing the data generator. In particular, the timing relationship between the clock and data outputs will directly influence circuit design as discussed below.

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For the parallel-load configuration, data is shifted into a 4-bit serial shift register (54S195) at 60 MHz as shown in the block diagram of Figure 1. (See Figure 8a for more detail). After every fourth serial shift, this register data is parallel-loaded into four sub-correlators so that the sub-correlators each operate at a rate of 15 MHz. The 54S195 is a fast 4-bit parallel access shift register ideal for use in the circuit, while TDC1023J 64-bit digital output correlator devices serve as the sub-correlators. (The 15 MHz operating rate is safely below the 20 MHz specified maximum rate of the TRW TDC 1023J devices.) A problem that arises is that of satisfying the required set up times for the 54S195 and TDC1023J circuits. The 54S195 requires that input data be present at least 5 ns before the rising edge of the register's clock. Since data from the MG-302 follows 1 or 2 ns behind the rising edge of the corresponding clock pulse out, the proper set up may be realized simply by delaying the 60 MHz clock. Passing the clock signal through two fast inverters (54S04) accomplishes this.

A logic circuit diagram for the latches and the sub-correlator clock is shown in Figure 2. An associated timing diagram appears in Figure 3. For the TDC1023J, latches must be used to acquire and hold data at the correlation register inputs at least 25 ns before the correlators are clocked to accept the new data. These latches must be fast enough to acquire the data within the interval that the data is valid, i.e., after each synchronous fourth clock pulse and before the next pulse which begins the next series of shifts. Suitable for use as latches are the high-speed JK flip-flops of the 54S112.

The divide-by 4 counter used to generate the 15 MHz clock may also be constructed using two of the 54S112 flip-flops in a Gray code synchronous counter configuration. This structure is superior to both the ripple counter configuration and the standard synchronous binary counter form because in a transition from any state to the next, only one flip-flop output changes. Eliminating the 01 to 10 transition in which both flip-flop outputs change increases performance reliability, especially at high clock rates. The 15 MHz clock signal used to clock the JK setup latches and sub-correlators can be formed from a state of this synchronous divide-by-4 counter. The TDC1023J circuits require a clock pulse width of 15 ns, while the setup latches require clock pulse widths of 6 ns. Forming the 15 MHz clock, therefore, involves gating together one output from each counter flip-flop and does not involve the original 60 MHz clock. The resulting 15 MHz clock pulses have widths of about 16.7 ns. Since there is a delay before the 15 MHz clock signal can actually clock the JK setup latches, the 15 MHz clock pulses are derived from the divide-by-4 counter state prior to each synchronous fourth pulse of the 60 MHz clock. The JK setup latches will then be clocked during the interval in which the data is valid. The 15 MHz clock is further delayed by 16 ns using delay gates, as shown in Figure 2, to satisfy the TDC1023J's setup time before clocking the sub-correlators.

III. MULTIPLEXED CORRELATOR OUTPUT CIRCUITRY

Obtaining the output of this multiplexed correlator requires two stages of binary adders as shown in Figure 1. The adders must keep pace at a rate of 15 MHz which implies add times of less than 66.67 ns. Although this requirement is much less demanding than the requirements of the serial-load schemes, which need add times of less than 16.67 ns, it is still a good idea to use fast adders. In either case, the most important goal is to make sure no inputs of a particular adder stage change until after the adder output sum corresponding to the present inputs, becomes available.

The 54S283 is a 4-bit binary parallel adder which when configured as an 8-bit adder, has a typical add time of 15 ns. As the fastest available TTL circuit of its kind, the 54S283 is suitable for use in both the serial and parallel-load multiplexed correlator schemes. Implementation is straightforward, and details are shown in the final circuit diagram of Figure 8b.

IV. DATA SELECTOR CIRCUITRY

In the general case where synchronization with the input data is not assured, the overall correlation circuit would consist of k multiplexed correlators, one for each of the k synchronization possibilities. For 60 MHz operation, a particular multiplexed correlator output will be the valid output of the entire correlator circuit during the period in which it corresponds to the $k/60\text{MHz} = k/0.06$ nanosecond interval immediately following a change in the register contents of the multiplexed correlator's sub-correlators. The overall correlation output can be formed by properly sampling each of the 9-bit outputs of the k multiplexed correlators. This requires data selector circuitry controlled by a k -bit ring counter that provides the k multiplexed correlator clock signals as described in reference 1.

For the cases in which k equals 2, 4, 8, or 16, the data selector can be implemented easily using readily available off-the-shelf TTL ALS multiplexers. Standard techniques can be used to design circuitry which will derive proper select inputs from the k -bit ring counter states. The design described here is for k equal to 4 and is illustrated in the circuit diagram of Figure 4.

In this case the 4 groups of 9-bit outputs may be thought of as 9 groups of 4, each group being composed of the 4 bits which occupy the same bit position in the four 9-bit outputs. The problem now is to permit the correct bit to pass through the circuitry at the correct instant. This may be accomplished conveniently with 4×1 multiplexers. Nine of these multiplexers are required, one for each correlation output bit position.

The select inputs can be derived from the states of the 4-bit ring counter in the following manner:

For the 4-bit ring counter: Q_D equals CK_1

Q_C equals CK_2

Q_B equals CK_3

Q_A equals CK_4 ,

where CK_1 is the clock for multiplexed correlator 1.

For a 4 x 1 MUX:

s_1	s_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Connect output bits from sub-correlator 1 to I_0 inputs

"	"	"	"	"	"	2	"	I_1	"
"	"	"	"	"	"	3	"	I_2	"
"	"	"	"	"	"	4	"	I_3	"

The desired states are then

Q_D	Q_C	Q_B	Q_A	Y	s_1	s_0
1	0	0	0	I_0	0	0
0	1	0	0	I_1	0	1
0	0	1	0	I_2	1	0
0	0	0	1	I_3	1	1

or more simply just,

Q_C	Q_B	Q_A	s_1	s_0
0	0	0	0	0
1	0	0	0	1
0	1	0	1	0
0	0	1	1	1

Thus by inspection,

$$s_1 = Q_A + Q_B$$

$$s_0 = Q_A + Q_C$$

Of course, for a larger k , the select inputs will be generated by "OR"ing a greater number of ring counter elements resulting in more than one level of gates.

For correct operation, the timing characteristics of the multiplexers and the combinational circuitry which determines the select inputs must be fast enough to permit switching at a rate of 60 MHz. A 54S195 may be used for the 4-bit ring counter, while the new 54ALS153 Dual 4-to-1 Multiplexer provides the only TTL data selector circuitry available today with switching speeds fast enough for this application. A problem which really cannot be resolved until actual implementation and testing is that of providing adequate and precise delays for the select input signals to s_1 and s_0 . These signals must be delayed long enough to reach the multiplexers after the correlation output corresponding to the same clock period but before the output for the next clock period. The valid interval is about 16.67 ns long. The estimated delay time necessary for these signals in the parallel-load scheme is between 105 ns and 115 ns. It is recommended, however, that such a parameter be determined through testing and measurement on the actual circuit.

V. PATH SELECTOR CIRCUITRY

Prior to operation, the proper paths must be implemented for data and clock pulses to be directed to the appropriate sub-correlator inputs to the Signal register (A_{in}), Reference register (B_{in}) and Mask register (M_{in}). (The Mask register can be used to shorten the effective correlator length by placing logic "0"'s in those bit positions to be neglected in performing correlation.) A divide-by-64 Enable signal needs to be generated to indicate whether one desires 64 clock pulses for register loading or a continuous clock for the correlation process. This path selector circuitry is illustrated in Figure 5. The four switches are implemented easily using a DIP switch. The AND gates are 54LS08 units and the inverters are 54LS04 units.

VI. SYNCHRONIZATION

Given the divide-by-64 Enable signal, it is a simple matter to configure a circuit such that when the divide-by-64 Enable signal is at the high logic level, only 64 pulses at 15 MHz will clock the sub-correlator registers chosen by the path selector switches. Figures 6a and 6b show this part of the multiplexed correlator. After 64 pulses are counted, the JK flip-flop toggles so that the 15 MHz Enable signal becomes a logic "0" shutting off the divide-by-4 counter before another pulse is generated.

For experimental test purposes an asynchronous reset button with a clean, reliable trigger for loading registers and starting the correlation process is required. The reset button can be constructed by connecting the CLEAR inputs of the JK set up latches, divide-by-4 counter, and JK toggle flip-flop to the same switch, so pressing the button sets these CLEAR inputs temporarily to logic "0". This results in the JK set up latches being cleared and both the divide-by-4 and divide-by-64 counters being reset. A good trigger for initiating the load or correlation process is a single pulse manually triggered from a pulse generator as mentioned in Section II. Such a pulse can be used to trigger the data generator that emits input data as well as the 60 MHz clock. It can also be used to toggle the 15 MHz Enable signal to an active

high state and could provide a pulse which, after a delay, may be used as the Load Reference (LDR) pulse needed to transfer a reference word from the TDC1023J's B register to its R register. Figure 7 shows the set up for these signal generators.

VII. EXPERIMENTAL CIRCUIT OPERATION

Figure 8a is a block diagram of the high speed multiplexed correlator circuit design and Figure 8b shows a pin diagram for it. Where synchronized input data is not available and $k = 4$ synchronization possibilities exist, four multiplexed sub-correlators like those in Figure 8a are required to present inputs to the data selector of Figure 4. Once the circuit is ready for operation, the following procedure should be used:

1. Reset circuit
2. Set desired data generator code
3. Reset data generator
4. Set path selector switches:

	<u>Load M</u>	<u>Load R</u>	<u>Correlation</u>
SW ₁	Off	Off	On
SW ₂	Off	On	Off
SW ₃	On	Off	Off
SW ₄	On	On	Off

5. Reset circuit
6. Trigger pulse generator

Note that this circuit should be reset twice: the first time to stop previous operation (if necessary) and the second time to clear out any changes caused by noise in setting the path selector. In loading the Reference or Mask registers of the sub-correlators, the circuit clock and data inputs from the data generator need not be of finite duration since setting the correct path selector switch will automatically stop any clocking of data into the sub-correlators after the first 64 clock pulses. The divide-by-64 counter disables the 15 MHz clock after 64 clock pulses. It is, therefore, possible to keep the data generator in the same output mode (CONTINUOUS/RUN) for both loading and correlating processes.

VIII. SUMMARY AND CONCLUSIONS

In theory, the parallel-load architecture that permits high speed digital correlation will have maximum correlation rates as determined by the maximum correlation speed of the sub-correlator devices. Practical limits, however, are defined by required clock pulse widths and maximum clock frequencies of the necessary supporting flip-flops and registers.

The primary consideration in designing the synchronized 64 x 4 bit parallel-load multiplexed correlator to operate at 60 MHz is that of satisfying the input data set up times for both the 4-bit shift register and the sub-correlator data registers. The shift register set up time is satisfied by delaying the register clock by an amount dependent on the timing relationship

between the data output and clock output of the particular data generator used. The subcorrelator register inputs are each preceded by a fast JK flip-flop that acts as a data latch by quickly acquiring data and holding it long enough to satisfy the set up requirements.

Synchronous operation is largely ensured by the synchronous starting of the divide-by-4 counter and the divide-by-64 counter. A reset button that brings the CLEAR inputs of the JK set up latches, divide-by-64 counter, and JK toggle flip-flop to a temporary low logic level, serves to reset the entire circuit. A single shot pulse serves to trigger the circuit operation. Even in the more general asynchronous case with $k=4$, the data selector circuitry involves the use of fast switching multiplexers which must be synchronized with the rest of the circuit through precise signal delays.

Future work on this project will have to be concerned with accurate measurement of propagation delays in the circuit. This information is necessary to enable proper evaluation of circuit operation. There is also a need for further consideration of circuit packaging requirements. Portions of this design have been breadboarded and verified in the laboratory. An experimental model of the entire circuit will be implemented and tested at a later date when adequate manpower is available.

IX. ACKNOWLEDGMENTS

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2. TRW LSI Products Data Sheet 116C for TDC 1023J Digital Output Correlator (64 Bit), El Segundo, CA, Sept 1980.

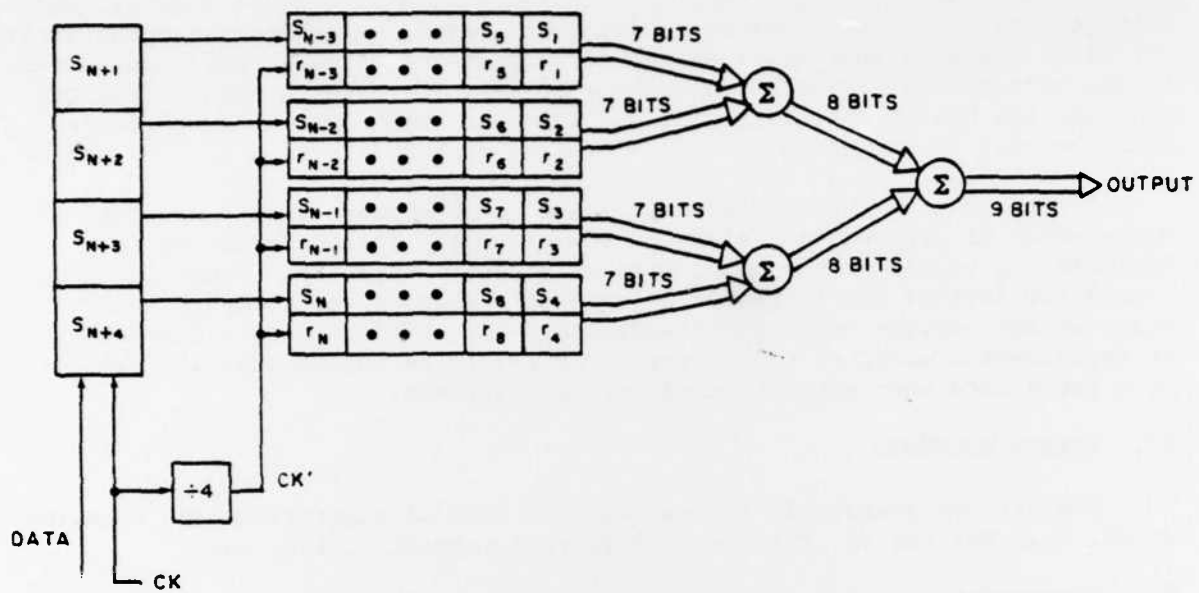
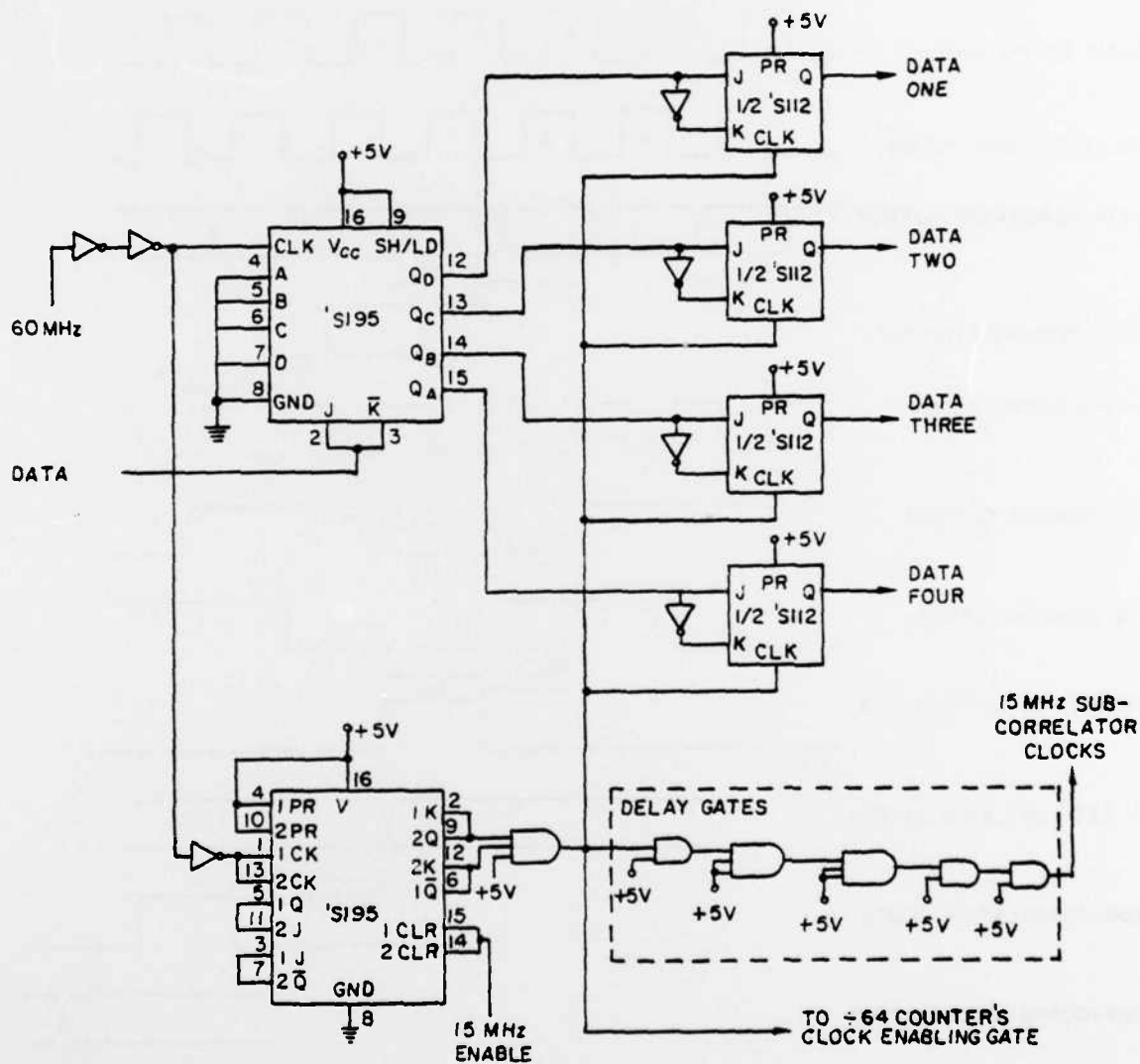


Fig. 1 — Parallel-load multiplexed correlator ($k = 4$)



NOTE: 'S195 INDICATES 54S195

Fig. 2 — Circuit diagram for parallel-load latch and sub-correlator clocks

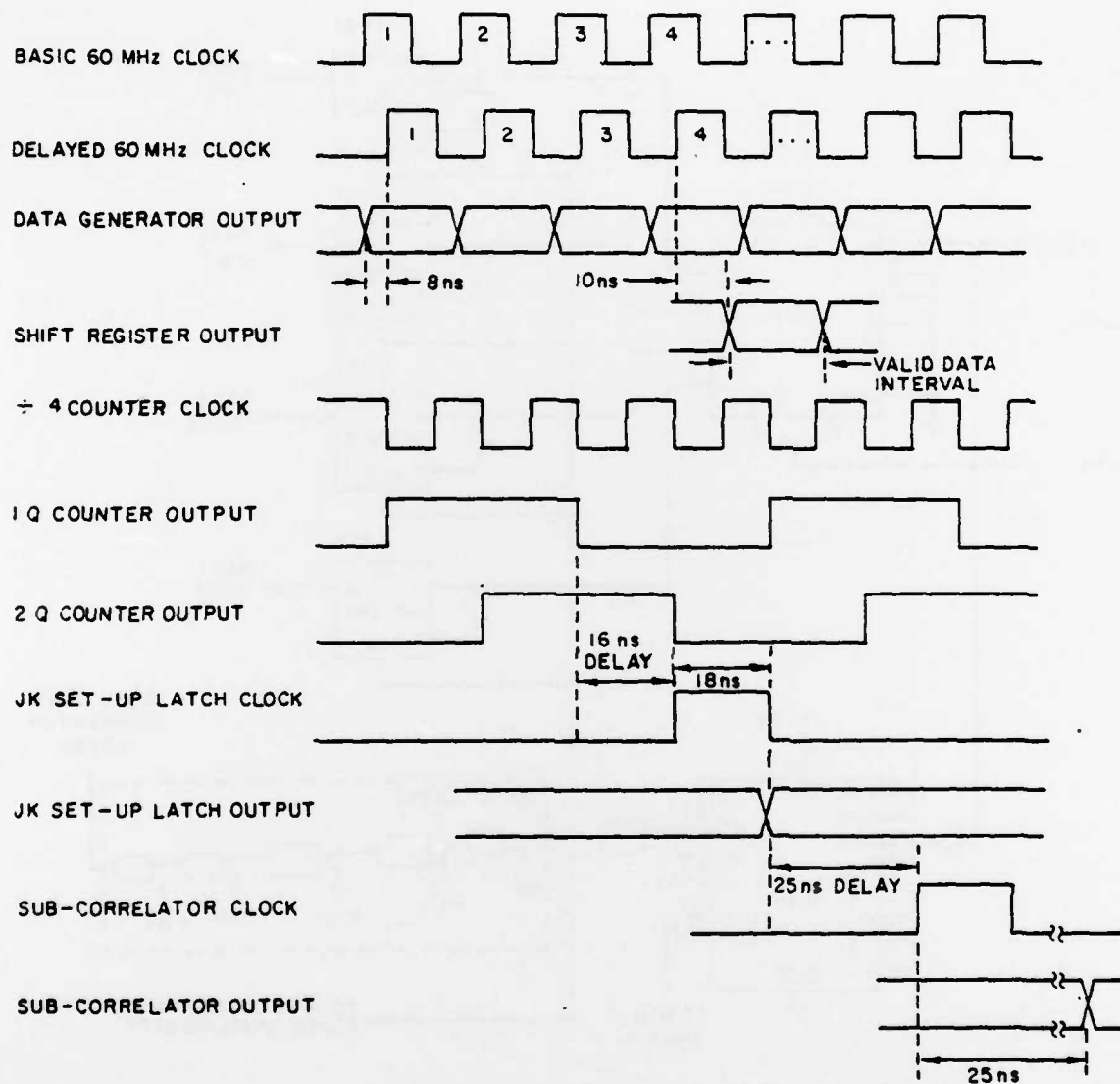


Fig. 3 — Timing diagrams for parallel-load multiplexed correlator

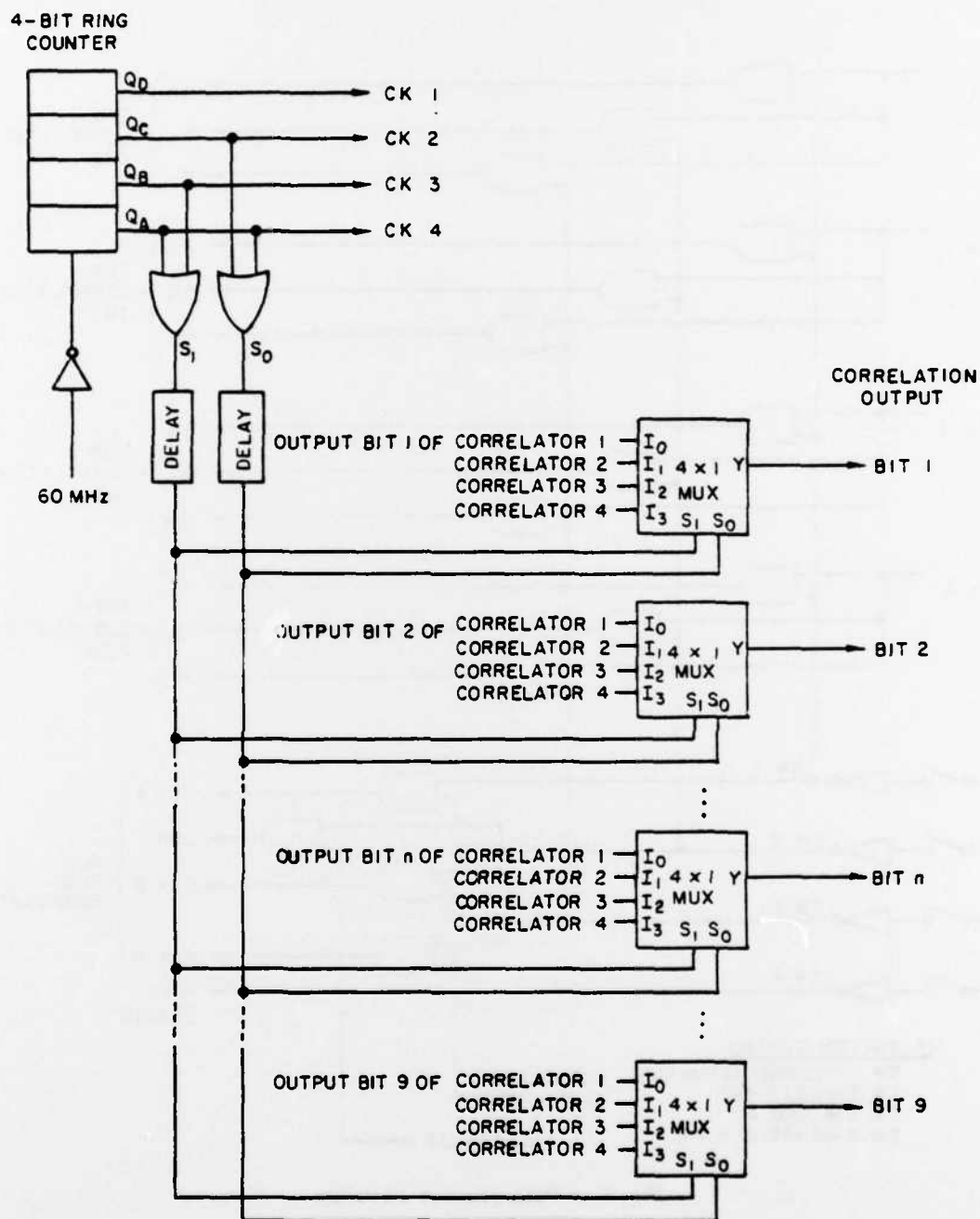


Fig. 4 — Data selector for $k = 4$ correlator

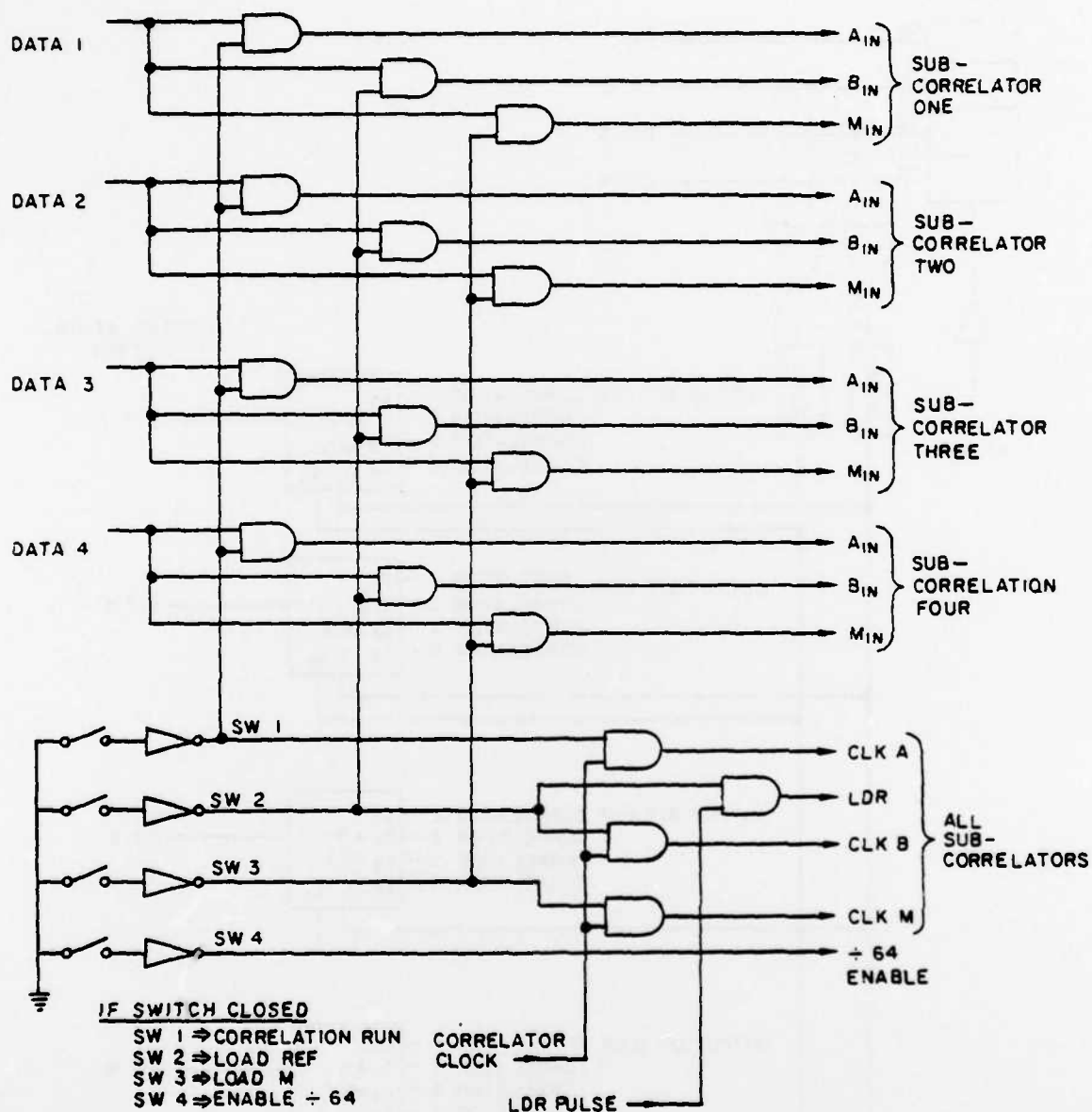


Fig. 5 — Path selector circuitry

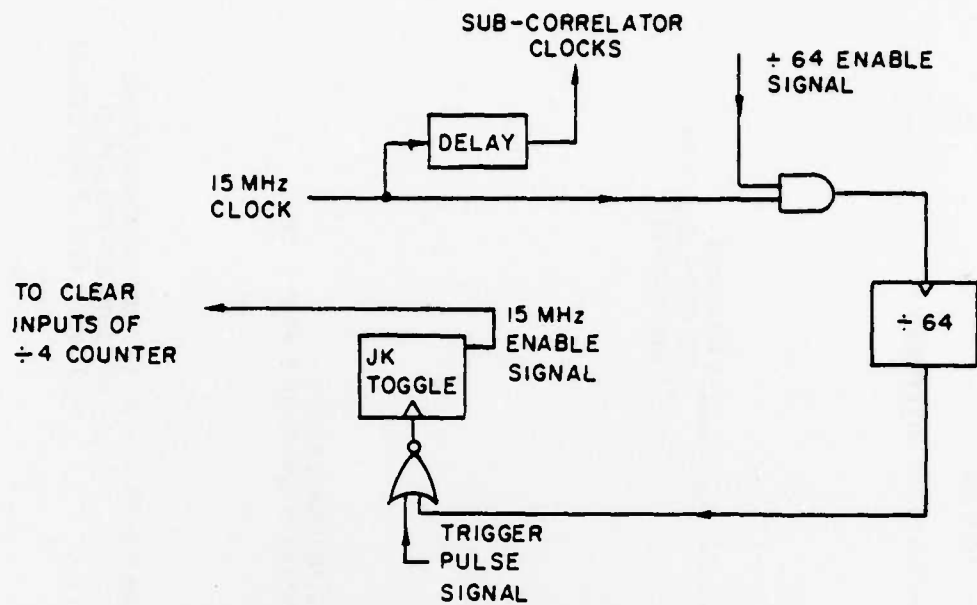


Fig. 6(a) — Block diagram of synchronous $\div 64$ circuitry

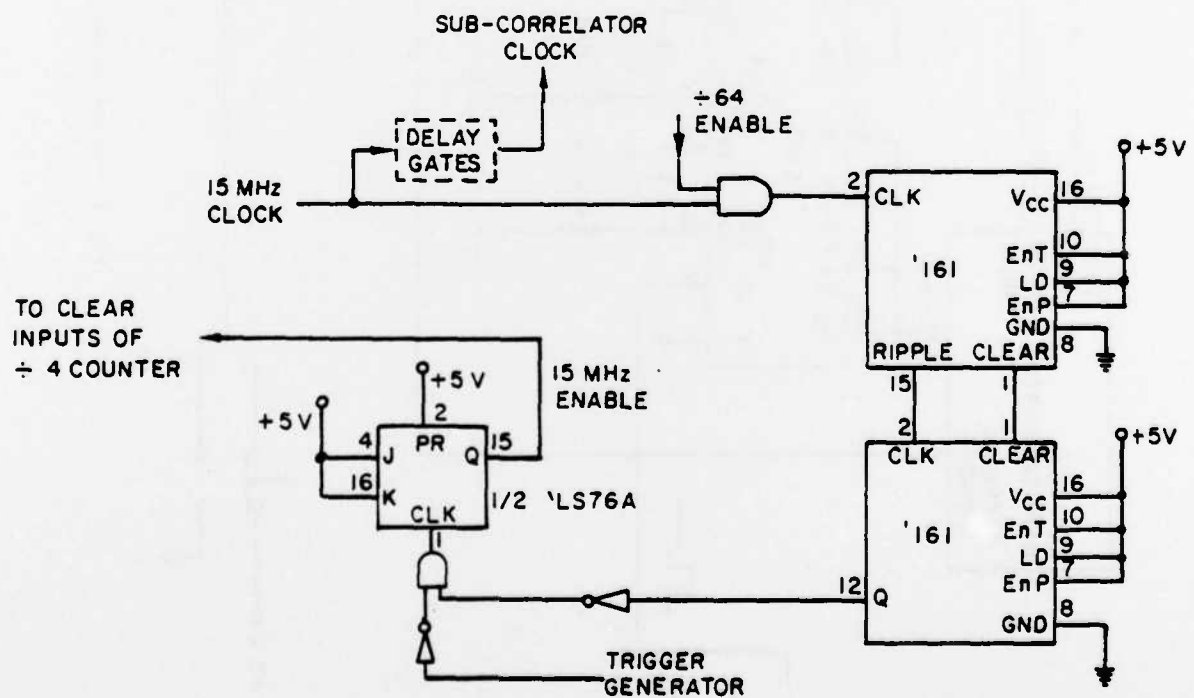


Fig. 6(b) — Circuit diagram for $\div 64$ synchronous counter

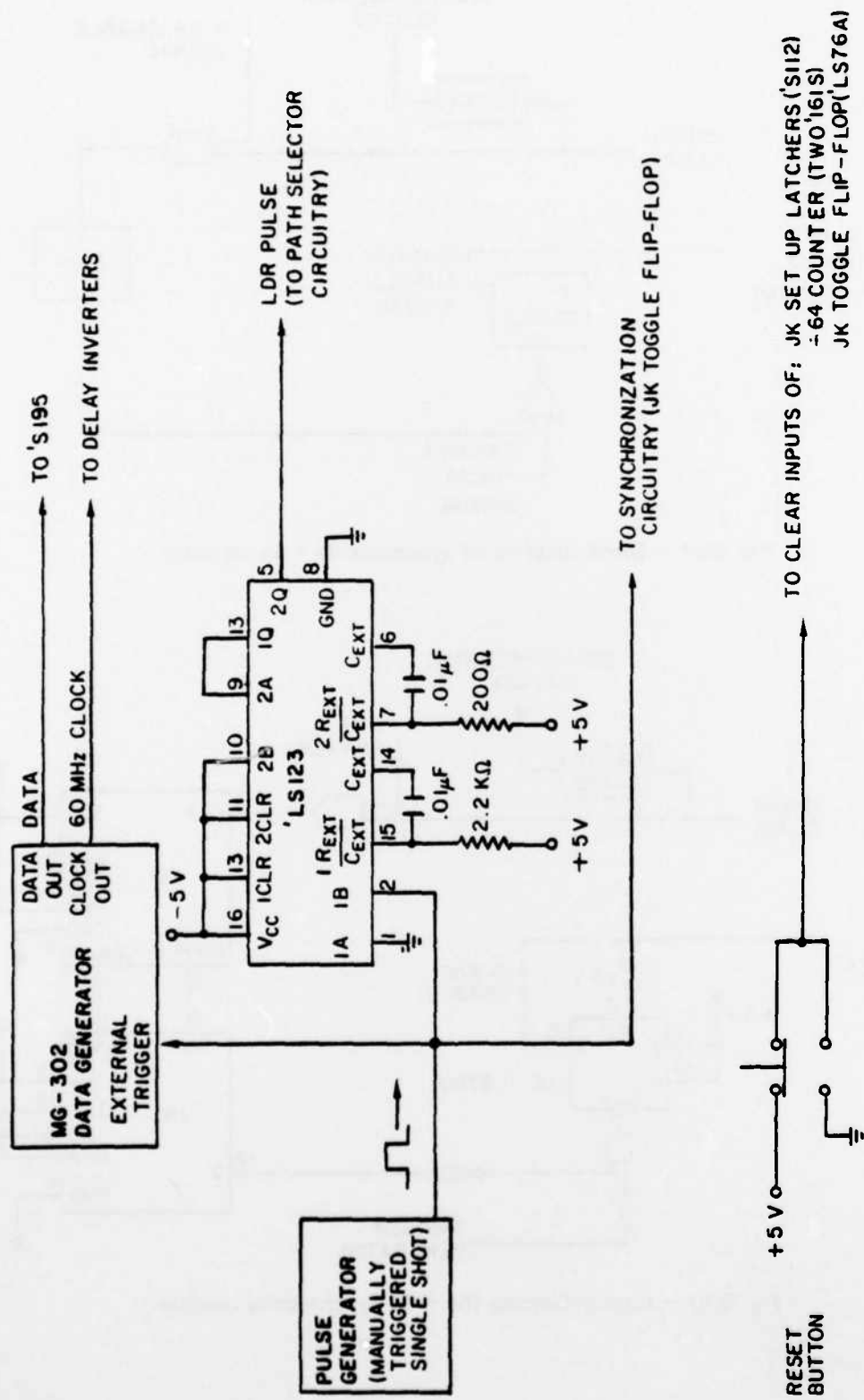


Fig. 7 — Input signal generators

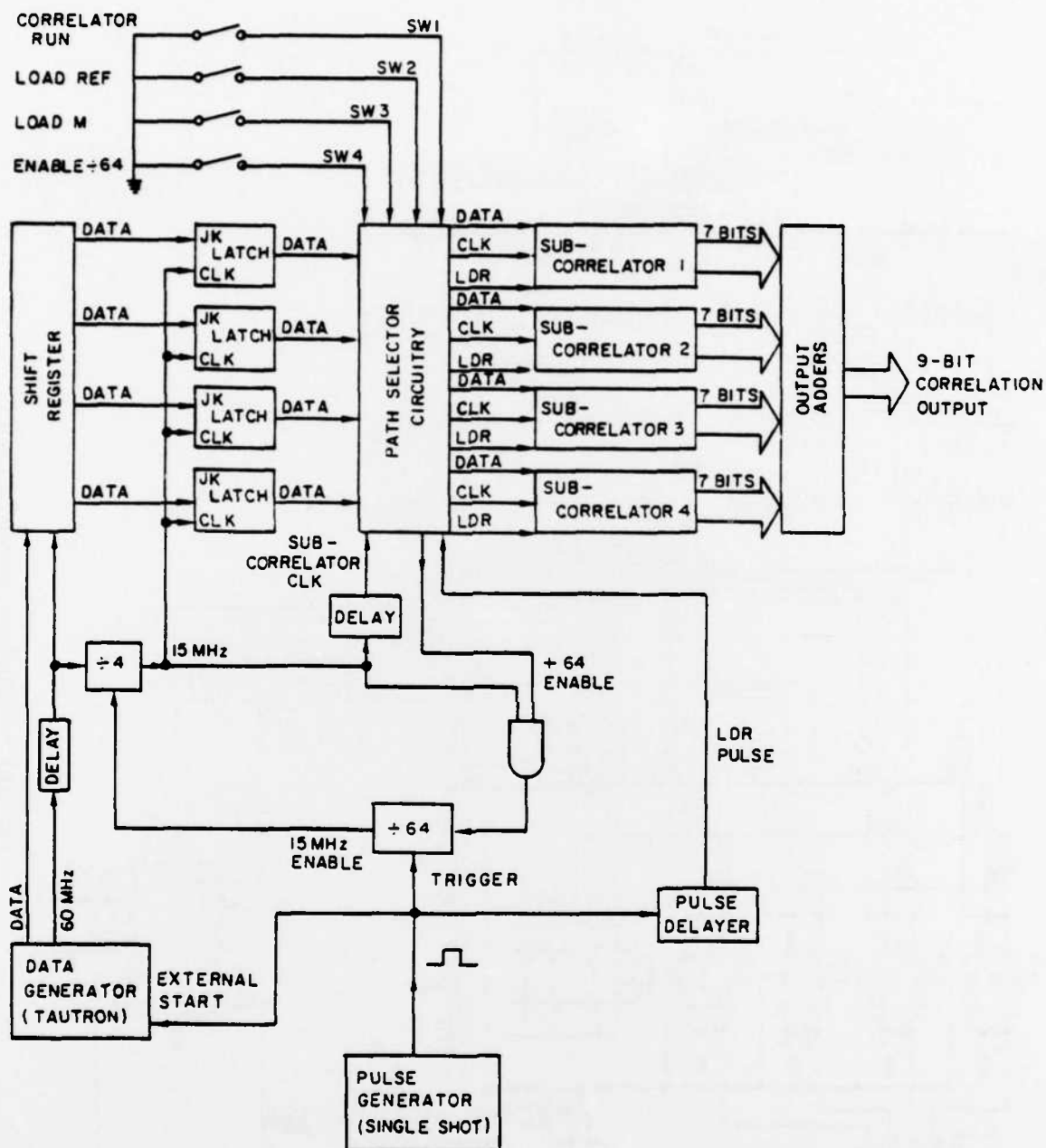


Fig. 8(a) — Block diagram of multiplexed correlator circuit

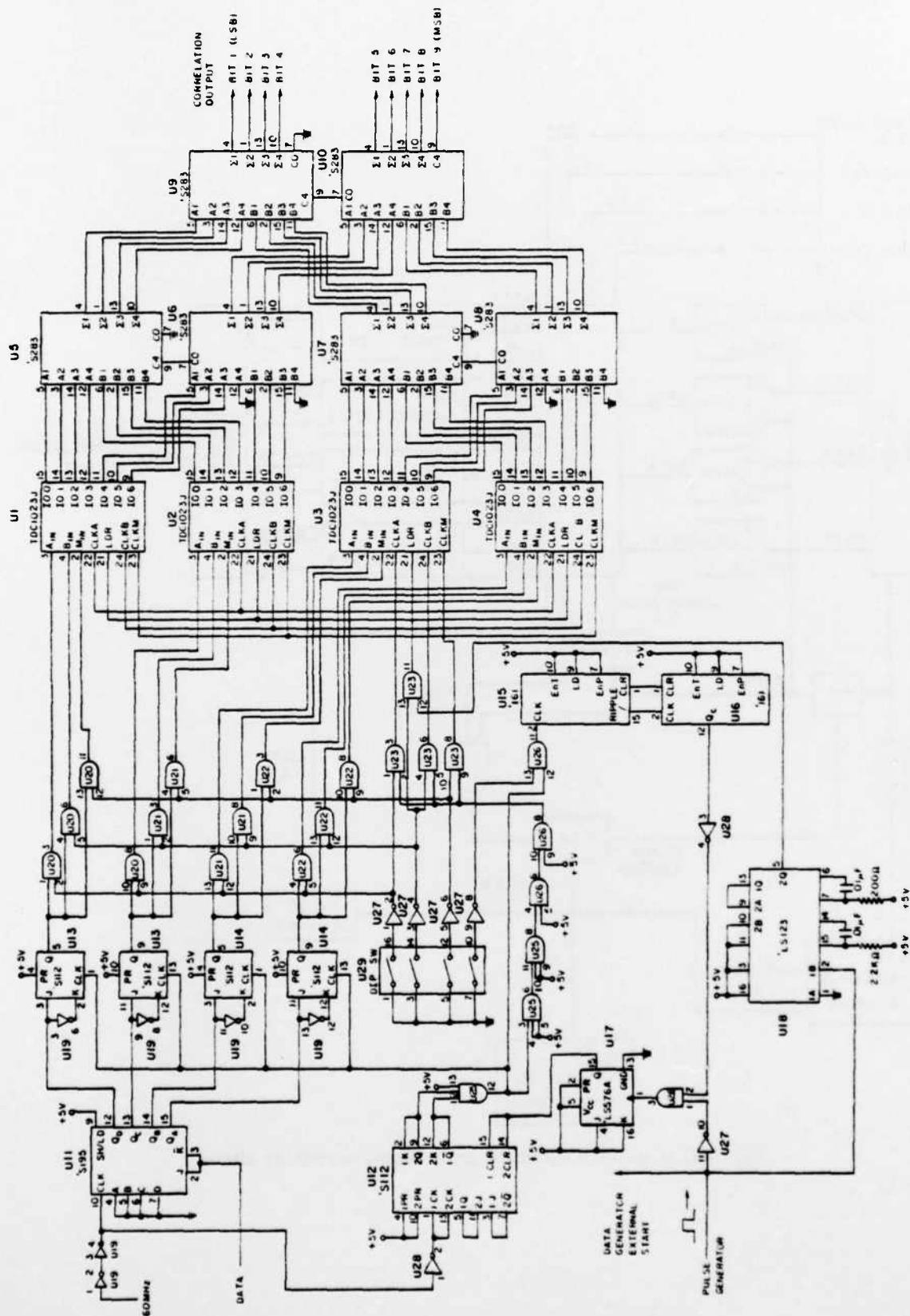


Fig. 8(b) — Multiplexed correlator circuit
(Reset lines not shown)

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